OIPE
JUN 16 2006
PATENT & TRADEMARK OFFICE
IAP35

Replacement Sheet

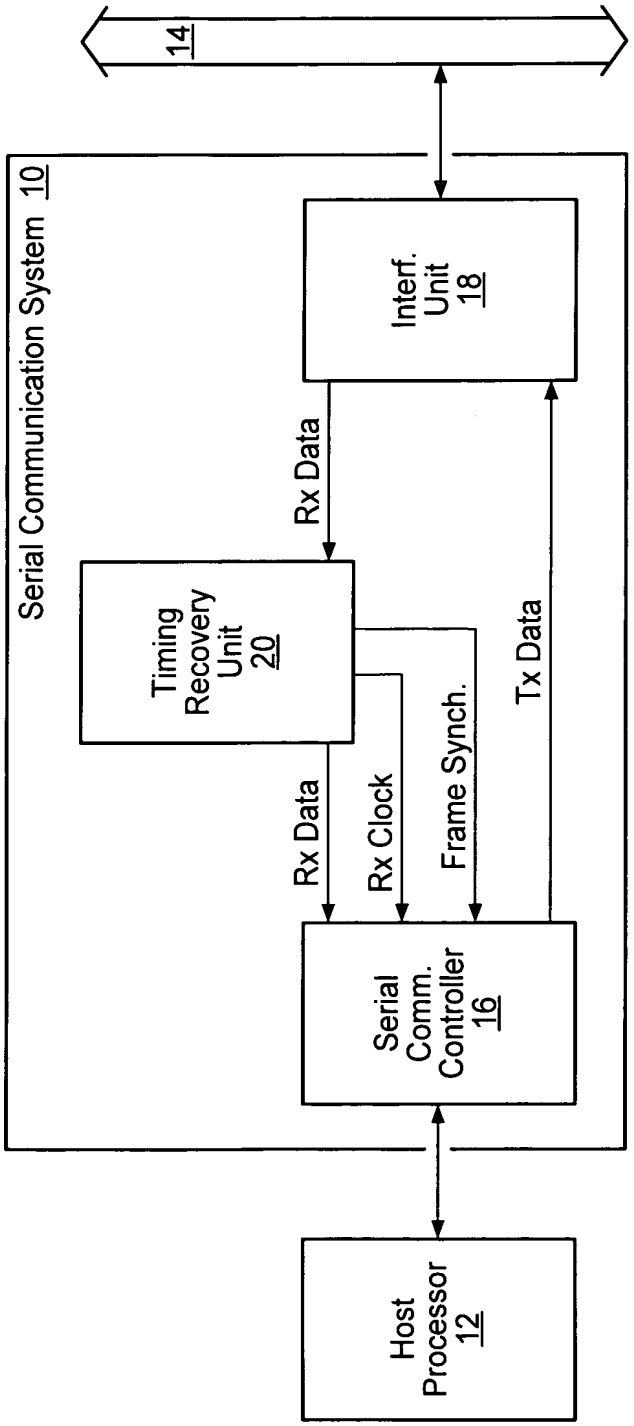

FIG. 1

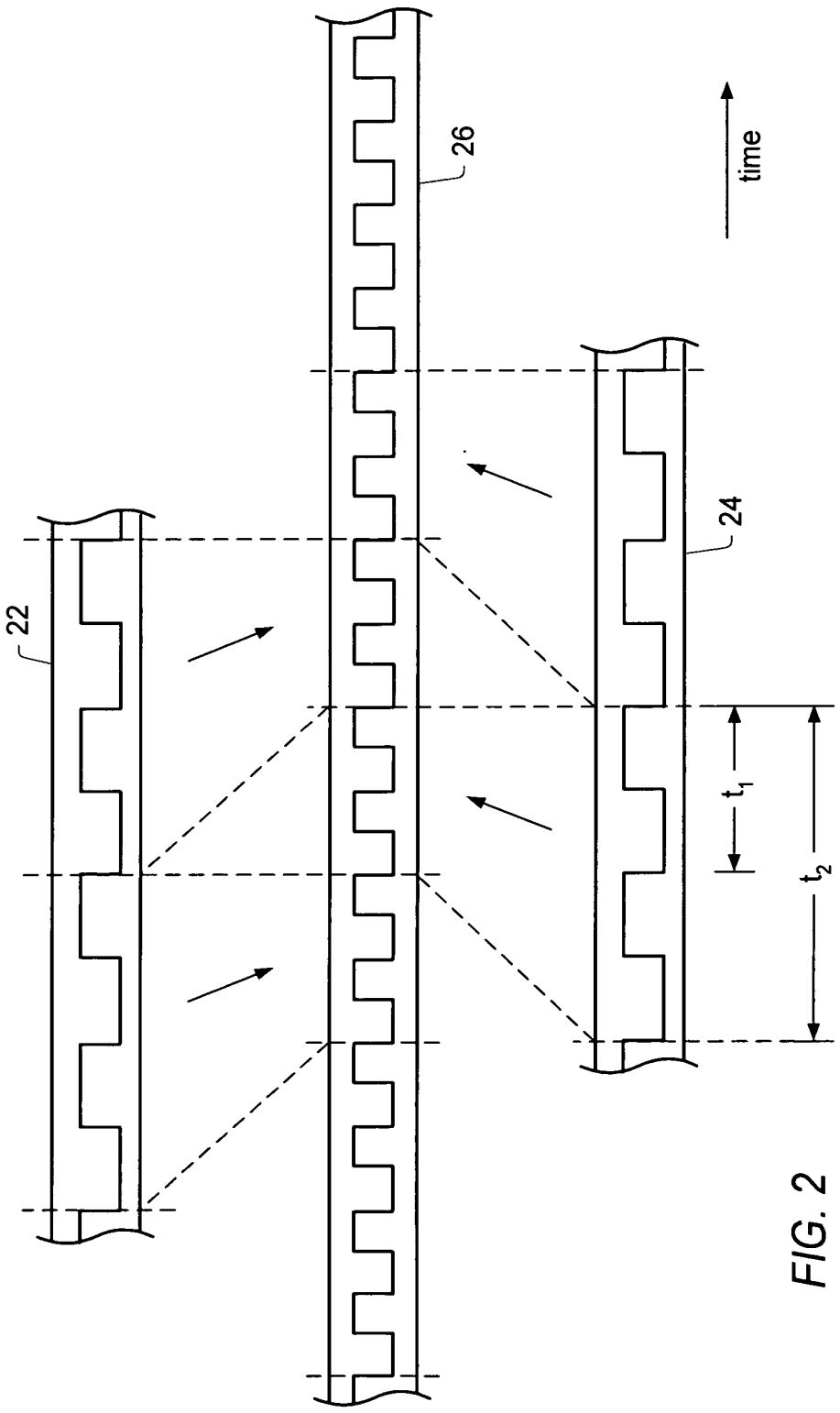

FIG. 2

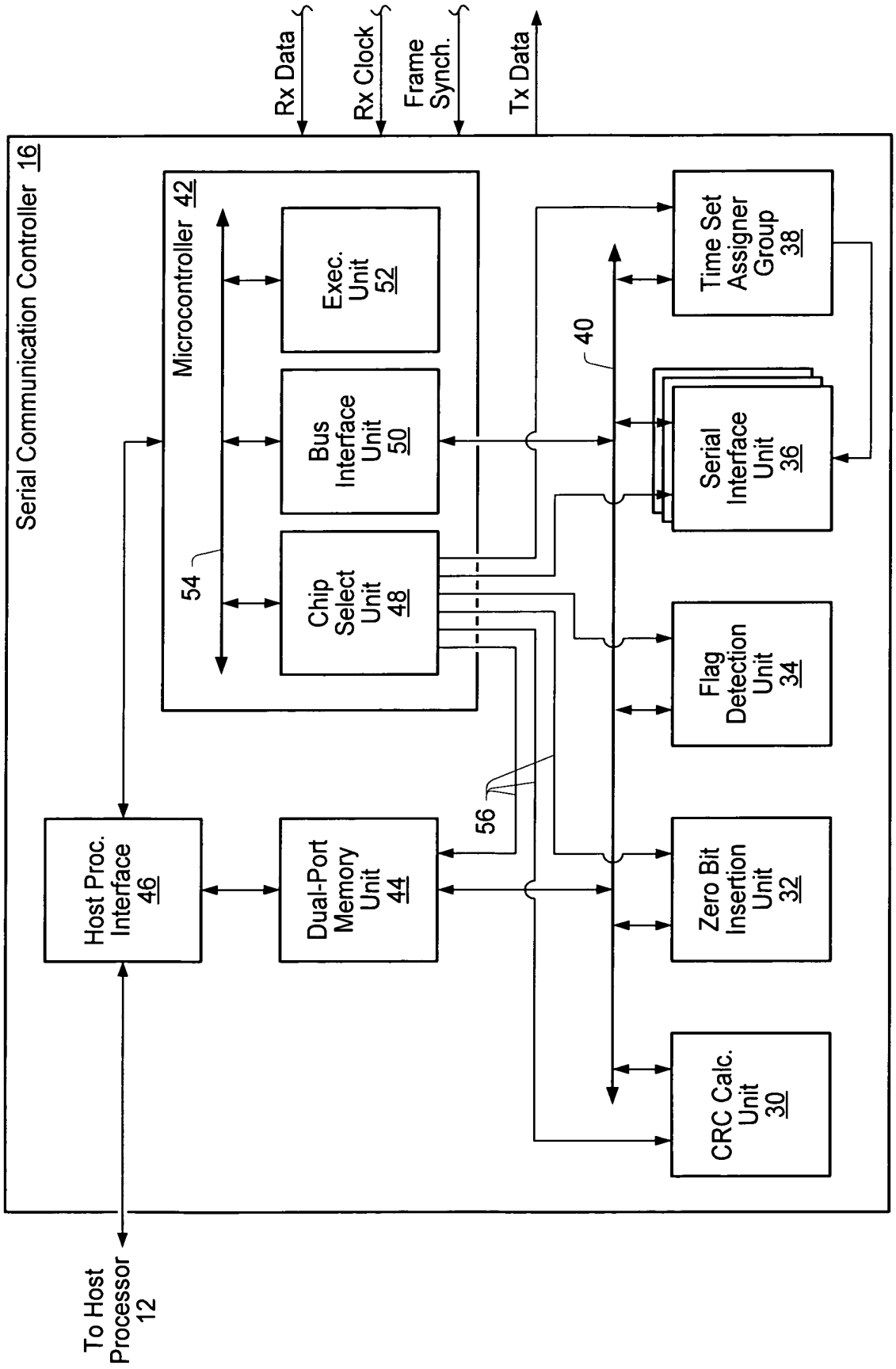
Rx Data
Rx Clock
Frame Synch.
Tx Data
Serial Communication Controller 16
Microcontroller 42
Exec. Unit 52
Bus Interface Unit 50
Chip Select Unit 48
54
40
Time Set Assigner Group 38
Serial Interface Unit 36
Flag Detection Unit 34
Zero Bit Insertion Unit 32
CRC Calc. Unit 30
Host Proc. Interface 46
Dual-Port Memory Unit 44
56
To Host Processor 12

FIG. 3

Opening Flag Field	Address Field	Control Field	Information Field	Frame Check Sequencing Field	Closing Flag Field
01111110	8 bits	8 bits	8*n bits	16/32 bits	01111110

FIG. 4

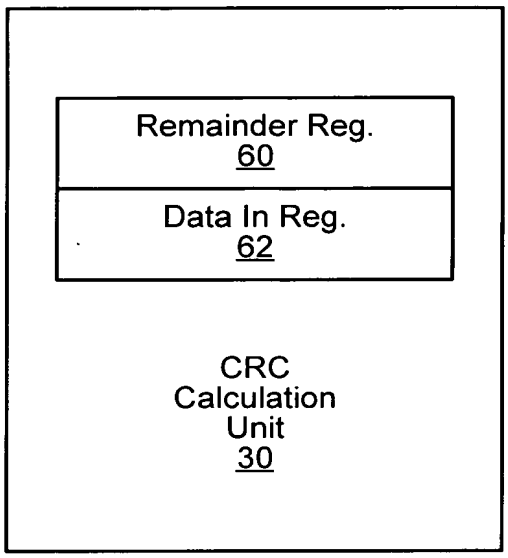
Remainder Reg.
60
Data In Reg.
62
CRC
Calculation
Unit
30

FIG. 5

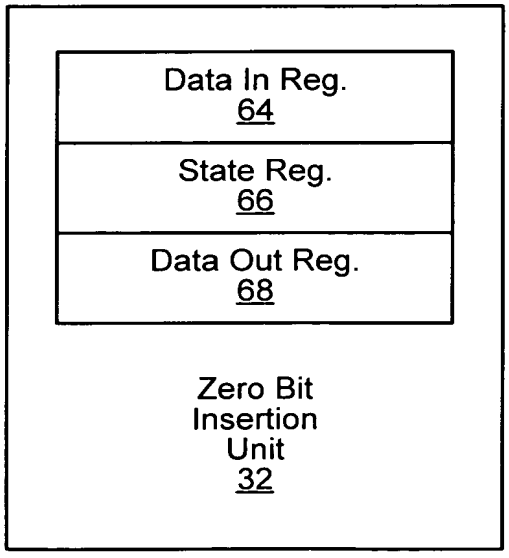
Data In Reg.
64
State Reg.
66
Data Out Reg.
68
Zero Bit
Insertion
Unit
32

FIG. 6

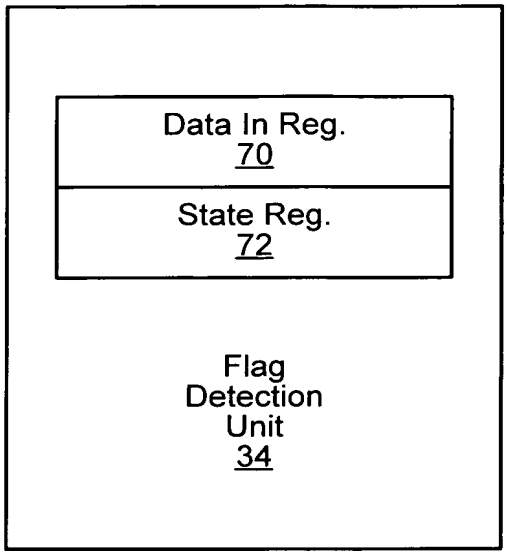
Data In Reg.
70
State Reg.
72
Flag
Detection
Unit
34

FIG. 7

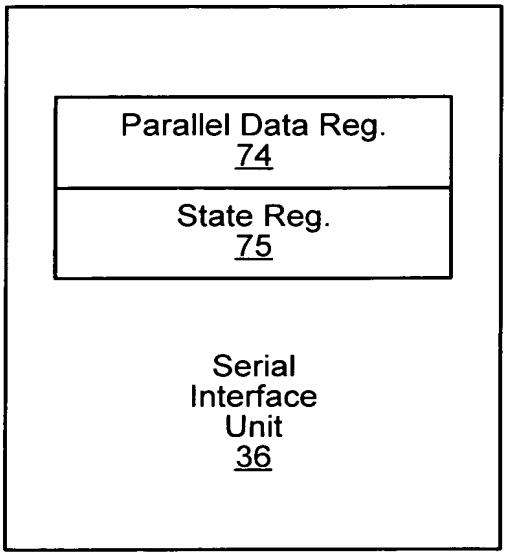
Parallel Data Reg.
74
State Reg.
75
Serial
Interface
Unit
36

FIG. 8

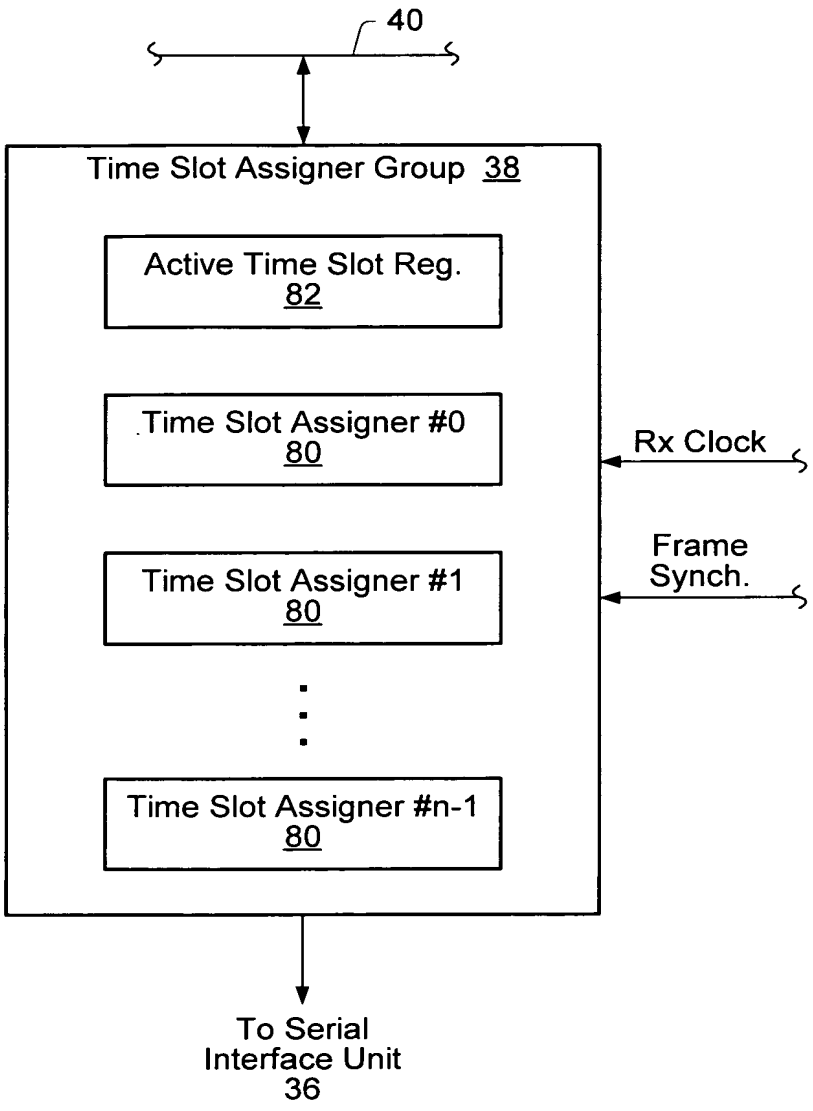
40
Time Slot Assigner Group 38
Active Time Slot Reg.
82
Time Slot Assigner #0
80
Time Slot Assigner #1
80
Time Slot Assigner #n-1
80
Rx Clock
Frame
Synch.
To Serial
Interface Unit
36

FIG. 9

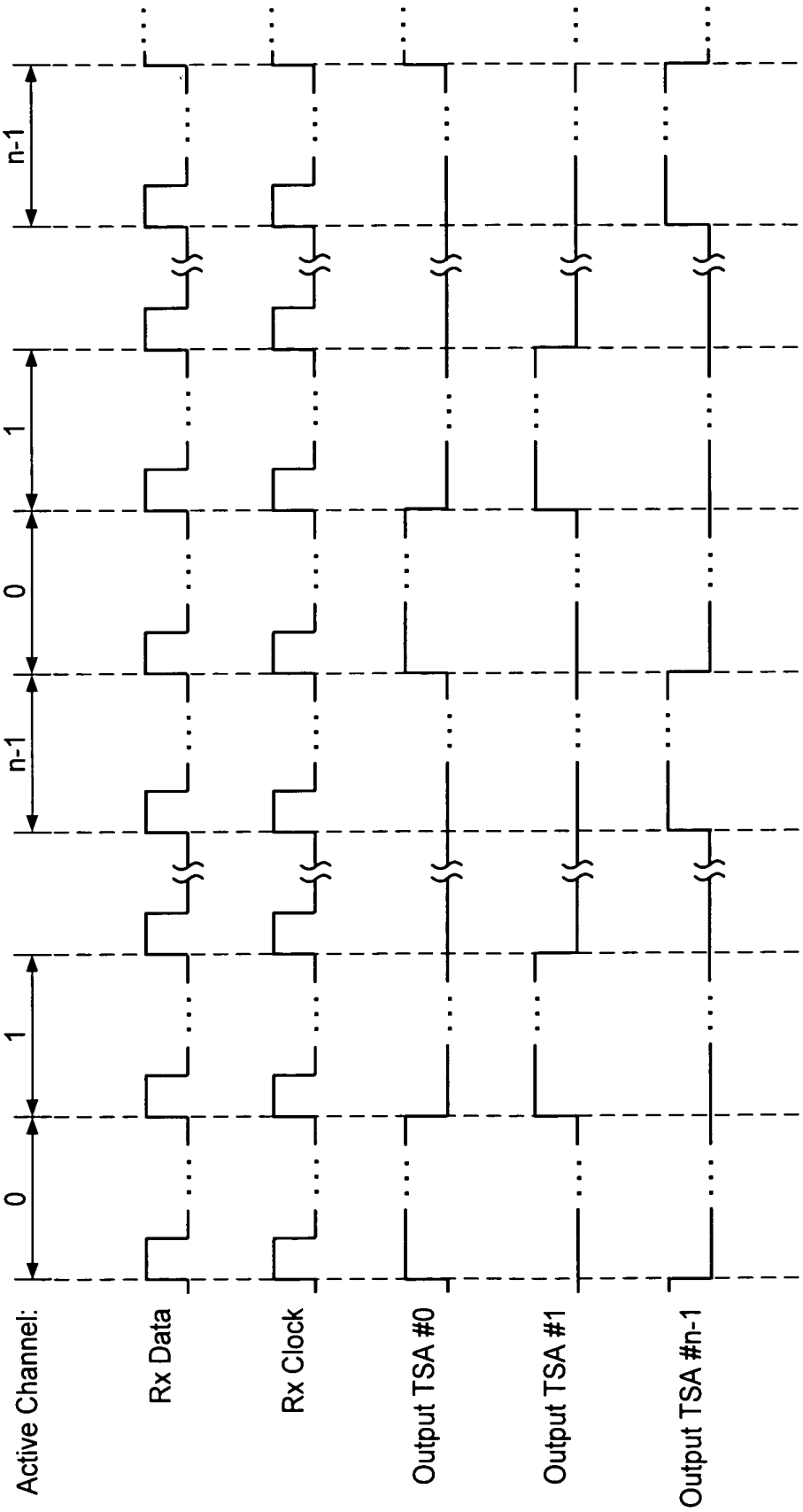
Active Channel:
Rx Data
Rx Clock
Output TSA #0
Output TSA #1
Output TSA #n-1
0
1
n-1
0
1
n-1
time

FIG. 10

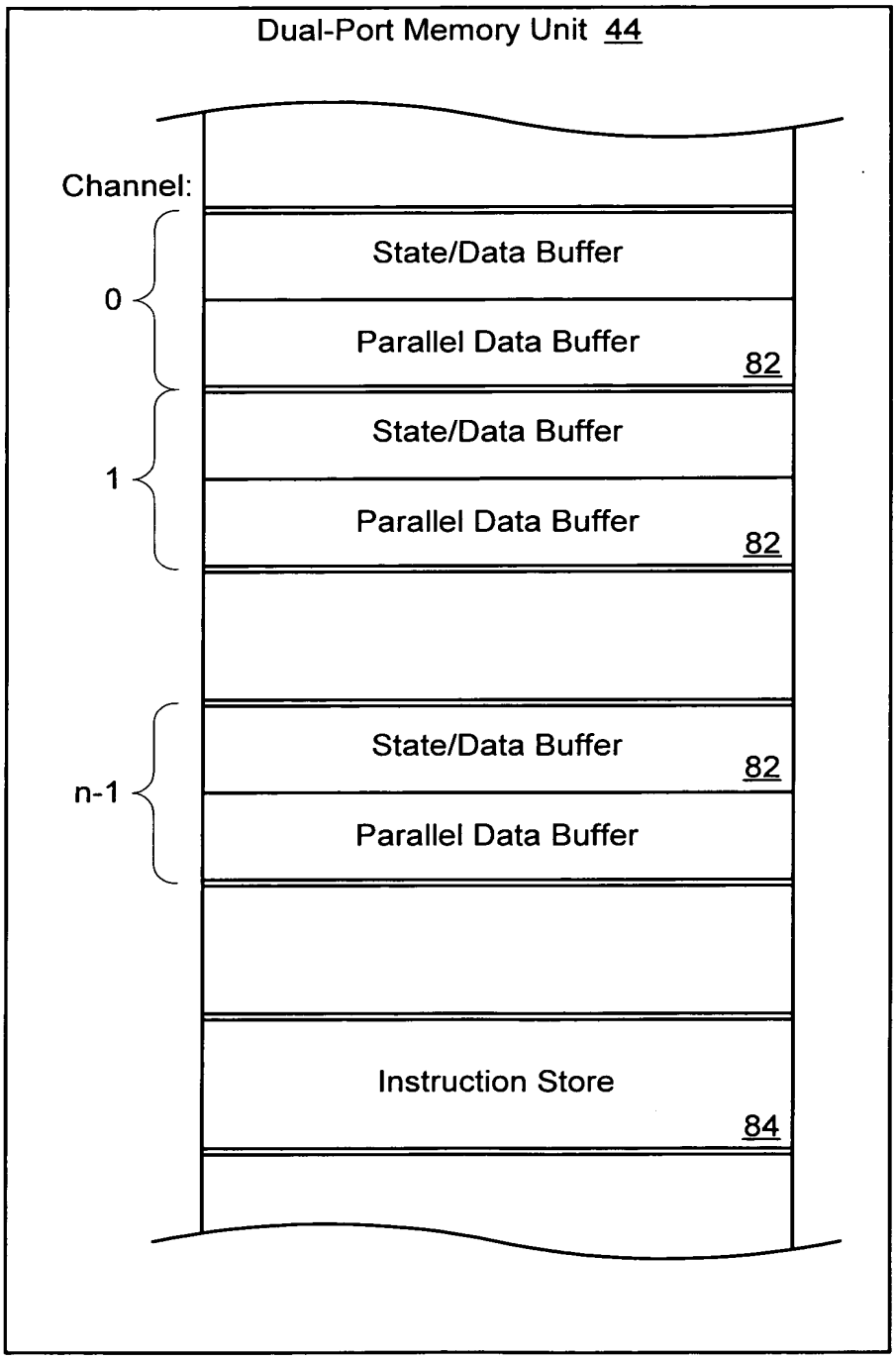
Dual-Port Memory Unit 44
Channel:
0
1
n-1
State/Data Buffer
Parallel Data Buffer
82
State/Data Buffer
Parallel Data Buffer
82
State/Data Buffer
82
Parallel Data Buffer
Instruction Store
84

FIG. 11